Enclosure – ECE/V

Department of Electronics and Communication Engineering (ECE)

School of Technology, PDPU

Vision:

To become a higher learning and research pioneer and to produce creative solutions using knowledge in the domain of Electronics and Communication Engineering to meet sustainable societal and environmental needs.

Mission:

- To deliver high-value education and strive for global recognition by excelling in teaching, research, and public service.
- To provide globally competent and futuristic graduates prepared for life-long engagement in the highly dynamic field of ECE.
- To develop engineering skills to meet futuristic technological challenges for sustainable environment, economy, and society.

Program Educational Objectives (PEOs):

- Prepare professionals with futuristic skills for industry, research organizations and academia in the field of electronics and communication engineering.
- Impart knowledge and technical skills to students for contribution to the design and development in Electronics, Communication and Signal Processing, and VLSI systems.
- Motivating graduates for lifelong learning with leadership qualities, ethics and life skills to become good human beings and engineering professionals.

Program Outcomes (POs):

The graduates of ICT department will be able to:

1. ***Engineering knowledge:*** Apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.

2. ***Problem analysis:*** Identify, formulate, review research literature and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and engineering sciences.

3. ***Design / development of solutions:*** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal and environmental considerations.

4. ***Conduct investigations of complex problems:*** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data and synthesis of the information to provide valid conclusions.

5. ***Modern tool usage:*** Create, select and apply appropriate techniques, resources and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. ***The engineer and society:*** Apply reasoning informed by the contextual knowledge to assess

societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. ***Environment and sustainability:*** Understand the impact of the professional engineering solutions in societal and environmental contexts and demonstrate the knowledge of and need for sustainable development.

8. ***Ethics:*** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. ***Individual and team work:*** Function effectively as an individual, and as a member or leader in diverse teams and in multidisciplinary settings.

10. ***Communication:*** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. ***Project management and finance:*** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work as a member and leader in a team, to manage projects in multidisciplinary environments.

12. ***Life-long learning:*** Recognize the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs):

The graduates of Electronics and Communication Engineering will be able to

- Apply electronics and communication engineering knowledge to solve multidisciplinary problems using tools and technologies.

- Understand, analyze and evaluate the impact of electronics and communication technology on Environment, Energy, Infrastructure, Organizations and Economy.

- Contribute to the environment, society and industries by providing solutions spanning Electronics, Communication and Signal Processing, and VLSI Systems.

Course Outline

Semester	Category Code	Course Name	Theory	Tutorial	Practical	Hrs	Credits
Semester I	PCC	Semiconductor Devices & Modelling	3	0	0	3	3
	PCC	Analog IC Design	3	0	0	3	3
	PCC	Digital CMOS VLSI Design	3	0	0	3	3
	PCC	Advanced Digital System Design	3	0	0	3	3
	PCC	IC Fabrication Technology	2	0	0	2	2
	PCC	Device Simulation Lab	0	0	2	2	1
	PCC	Analog IC Design Lab	0	0	2	2	1
	PCC	Digital IC Design Lab	0	0	2	2	1
	PCC	FPGA-based System Design Lab	0	0	2	2	1
	Project	Scientific Writing and Publication Ethics	2	0	0	2	2
			16	**0**	**8**	**24**	**20**
Semester II	**Category Code**	**Course Name**	**Theory**	**Tutorial**	**Practical**	**Hrs**	**Credits**
	PCC	Mixed-Signal VLSI Design	3	0	0	3	3
	PCC	Mixed-Signal VLSI Design Lab	0	0	2	2	1
	PCE	Professional Core Elective	3	0	2	5	4
	PCE	Professional Core Elective	3	0	0	3	3
	PCE	Professional Core Elective	3	0	0	3	3
	PCE	Professional Core Elective	3	0	0	3	3
	Project	Research Methodology	2	0	0	2	2
	Project	Seminar				0	1
			16	**0**	**4**	**21**	**20**

Semester III	**Category Code**	**Course Name**	**Theory**	**Tutorial**	**Practical**	**Hrs**	**Credits**
	Project	Project Phase - I					**13**
	Project	Summer Internship /IEP (6 Week)					**1**
			0	**0**	**0**	**0**	**14**
Semester IV	**Category Code**	**Course Name**	**Theory**	**Tutorial**	**Practical**	**Hrs**	**Credits**
	Project	Project Phase - II and Dissertation					**16**
			0	**0**	**0**	**0**	**16**
Total Credits (Semester I to IV)							**70**

Core Electives (Theory + Lab)	
Testing and Verification of VLSI Circuits	Testing and Verification of VLSI Circuits Lab
VLSI Physical Design	VLSI Physical Design Lab

Core Electives (Theory Only)
IC Manufacturing, Packaging & Testing
Low Power VLSI Design
VLSI Signal Processing Architecture
RFIC Design
Advanced VLSI Interconnects
Mechatronics & Control for Semiconductor Manufacturing
Linear Algebra and Optimization

Semester 1

<Course Code>					Semiconductor Devices & Modelling					
Teaching Scheme					Examination Scheme					
					Theory			Practical		Total
L	T	P	C	Hrs./Week	MS	ES	IA	LW	LE/Viva	
3	0	0	3	3	25	50	25	--	--	100

COURSE OBJECTIVES:

- To offer profound understanding of the fundamentals of semiconductor devices.
- To impart comprehensive knowledge of device technology.
- To provide a foundation in the physics and technology of semiconductor devices to address the challenges of modern electronic devices.

UNIT-1: FUNDAMENTALS OF SEMICONDUCTOR DEVICES **12 Hrs.** Review of semiconductor theory: Types of Semiconductors, Doing, Femi-levels, Poisson‟s equation, continuity equation, diffusion\drift model, velocity saturation, hot carriers, avalanche breakdown, punch through and kirk Effects, Einstein relation, Carrier generation and recombination, Semiconductor junctions: Schottky, homo- and hetero-junction band diagrams and I-V characteristics, Modeling of BJT: DC, small signal, high frequency and noise models of bipolar junction transistors. Extraction of BJT model parameters. Ebers-Moll and Gummel- poon models.

UNIT-2: MOS TRANSISTOR **10 Hrs.**

MOSFET structure and its operation, MOS Capacitor, C-V Characteristics with frequency effects, Threshold voltage, Drift-Diffusion Approach for IV, Sub-threshold current and slope, Body effect, Pao & Sah Model, Detail 2D effects in MOSFET, Short channel effects, Velocity saturation, Hot electron effects, DIBL, GIDL, Ballistic transport, High K dielectric, Small-signal model, Single electron transistor (SET modelling).

UNIT-3: MOS MODELLING **10 Hrs.**

Models for metal-semiconductor contacts and heterojunctions. MOSFET - quantum theory of 2DEG, gradual channel approximation, charge control models, BSIM model, second-order effects. MESFET-Shockley, velocity saturation and universal models. HEFT - Basic and universal models. SPICE and small-signal models.

UNIT-4: MODERN SEMICONDUCTOR DEVICES **10 Hrs.**

MOS Transistor: Strained Si-FET, SOI MOSFET, FinFET, GAAFET, MBCFET. MOS Memory Devices and Sensors: SRAM, DRAM, Flash memory, Photodetector, Chemical sensors, Electronic noise, and its applications.

TOTAL HOURS: 42 Hrs.

COURSE OUTCOMES:

On completion of the course, the student will be able to:

CO1: Get insight into basic concepts of semiconductors for better understanding of modern electronic devices.

CO2: Understand and analyze the various conduction mechanisms in semiconductor devices.

CO3: Observe and analyze the charge carriers‟ transport through visualizing energy band bending at metal/semiconductor and semiconductor/semiconductor junctions.

CO4: Assess the various issues of mos devices with size scaling and analyze the theoretical or mathematical models of mos transistors.

CO5: Identify and understand the various fabrication steps and processes of modern devices in the electronic industry.

CO6: Build upon the understanding to improve the modern semiconductor devices for specific desired applications with having proper understanding of device issues and constraints at research and industry levels.

TEXT/REFERENCE BOOKS:

1. Solid state electronic devices by b.g. streetman & s. Banerjee, phi.
2. Semiconductor physics and devices by donald a. Neamen, 4th edition, mhe.
3. Silicon vlsi technology by j. D. Plummer, m. D. Deal & p. B. Griffin, prentice-hall, 2000.
4. Finfets and other multi-gate transistors, by p. Colinge, springer 2009.

<Course Code>					Analog IC Design					
Teaching Scheme					Examination Scheme					
L	T	P	C	Hrs./Week	Theory			Practical		Total Marks
					MS	ES	IA	LW	LE/Viva	
3	0	0	3	3	25	50	25	--	--	100

COURSE OBJECTIVES

- To understand analysis and design of MOSFET-circuits, current mirrors, and feedback.
- To understand analysis and design of CMOS operational amplifiers.
- To understand analysis and design of CMOS oscillators.

UNIT I: MOSFET-CIRCUITS CONFIGURATIONS AND CURRENT MIRRORS **12 Hrs.**

Introduction to MOSFETs, MOSFET-Circuits Configurations: Common-Source, Source Follower, Common- Gate, Cascode, and Basic Differential Pair; Current Mirrors: Basic Current Mirrors, Cascode Current Mirrors, and Active Current Mirrors; Biasing Techniques: CS Biasing, CG Biasing, Source Follower Biasing, Differential Pair Biasing

UNIT II: FEEDBACK **10 Hrs.**

General Considerations: Properties of Feedback Circuits, Types of Amplifiers, Sense and Return Mechanisms, Feedback Topologies: Voltage-Voltage Feedback, Current-Voltage Feedback, Voltage-Current Feedback, Current-Current Feedback, Effect of Feedback on Noise, Effect of Loading in Feedback

UNIT III: OPERATIONAL AMPLIFIERS **10 Hrs.**

Performance Parameters, Two- Stage Operational Amplifier (Op Amp) Design, Gain Boosting Op Amp Design, Comparison, Stability and Frequency Compensation in Op Amps

UNIT IV: OSCILLATORS **10 Hrs.**

General Considerations, Ring Oscillators, LC Oscillators, Voltage-Controlled Oscillators, Concept of PLL.

TOTAL HOURS: 42 Hrs.

COURSE OUTCOMES

On completion of the course, students will be able to:

CO1 : Identify large-signal and small-signal analysis of different MOSFET-based circuit configurations.
CO2 : Understand the current mirrors.
CO3 : Apply the CMOS feedback amplifier circuits.
CO4 : Analyze the design of application-specific CMOS operational amplifiers.
CO5 : Evaluate the design of robust and high-performance CMOS oscillators.
CO6 : Create the design of advanced analog integrated circuits as per the application-specific requirements.

TEXT/REFERENCE BOOKS

1. Behzad Razavi, “Design of analog CMOS integrated circuits,” 2nd edition, Mcgraw Hill, 2017.
2. J. Michael jacob, “applications and design with analog integrated circuits,” phi, 2nd edition, 2004.
3. Paul r. Gray, paul j. Hurst, stephen h. Lewis, robert g. Meyer, “analysis and design of analog integrated circuits,” 5th edition, wiley, 2009.
4. Sedra and smith, “microelectronic circuits,” oxford university press, 5th edition, 2005.

XXXX					Digital CMOS VLSI Design					
Teaching Scheme					Examination Scheme					
L	T	P	C	Hrs/Week	Theory			Practical		Total Marks
					MS	ES	IA	LW	LE/Viva	
3	0	0	0	3	25	50	25	--	--	100

COURSE OBJECTIVES

- To understand the characteristics and concepts related to the design of digital CMOS VLSI circuits/gates.
- To explore various CMOS logic styles, and design CMOS VLSI circuits/gates at the transistor level and layout level.
- To analyze the performance/power of digital CMOS VLSI circuits/gates.

UNIT 1 INTRODUCTION TO DIGITAL CMOS VLSI 08

Trends in VLSI/Semiconductor industry, related to technology (Moore's) scaling; ITRS Roadmap; Overview of semiconductor devices inherent in the MOSFET: MOSFET I/V Characteristics, MOSFET C/V Characteristics, Second Order Effects.

DC Transfer Characteristics: CMOS inverter DC Characteristics, Beta Ratio Effects, Noise Margins, Pass Transistor DC Characteristics

UNIT 2: Estimation of Delay and Power of CMOS Gates. 12

Delay: Various delays in CMOS gates, Delay Modelling, Propagation Delay: First-Order Analysis, Delay optimization using Logical Effort, Parasitic Delay reduction, Delay optimization in Multistage Logic Networks.

Power: Estimation of static and dynamic powers in CMOS gates, techniques to reduce the dynamic powers.

UNIT 3: Various Logic families and Sequential design 14

Combinational Design: Static CMOS design, Various pass transistor-based logic families, Ratioed logic, Design of Dynamic logic families, and their delay estimations

Sequential Design: Design of various Latches and flip-flops, Timing analysis of Sequential circuits: Max-Delay Constraints, Min-Delay Constraints, Time Borrowing, Clock Skew, Circuit Design of Latches and Flip-Flops

UNIT 4: VLSI subsystem design 8

Basic building blocks of arithmetic circuits: Carry ripple adders, various carry prefix adders, their advantages, and disadvantages. Comparators, array multipliers, shifters

Array subsystems: SRAM, Row circuitry, column circuitry, DRAM, NAND and NOR flash memory and other content addressable memories.

Total: 42 Hours

COURSE OUTCOMES

On completion of the course, student will be able to

CO1 - Identify the pros and cons, and the trends related to scaling of the CMOS VLSI technology.

CO2 - Understand the characteristics, sub-parts, and regions of operation of the MOSFET, and use their I-V equations.

CO3 – Design of the combinational and sequential circuits using digital CMOS VLSI standard gates and compound gates, at the transistor –level.

CO4 - Estimate the performance/power of digital CMOS VLSI standard and compound gates.

CO5 - Analyze and compare various digital CMOS logic styles and gates/circuits.

CO6 - Create layouts of digital CMOS VLSI standard gates and compound gates, based on Lambda rules.

TEXT/REFERENCE BOOKS

- Neil Weste, David Harris, Ayan Banerjee, "CMOS VLSI Design: A circuits and systems perspective", 3rd Edition, Pearson.
- Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits", 3rd Edition, Tata McGraw Hill.
- Robert F. Pierret, "Semiconductor Device Fundamentals", 1st Edition, Pearson.Prentice Hall.

<Course Code>					Advanced Digital System Design					
Teaching Scheme					Examination Scheme					
L	T	P	C	Hrs./Week	Theory			Practical		Total Marks
					MS	ES	IA	LW	LE/Viva	
3	0	0	3	3	25	50	25	--	--	100

COURSE OBJECTIVES

- To get an in-depth knowledge of digital system design.
- To analyse the different performance parameter (speed, power and area) of a digital system.
- To get an in-depth knowledge digital system design options and trade-offs.

UNIT 1: ADVANCED COMBINATIONAL AND SEQUENTIAL DESIGN **10 Hrs.**

Review of Combinational and Sequential logic design, BDD, ROBDD, Moore and Mealy machine, Design of synchronous sequential circuits – state diagram, state table, state table assignment and reduction, designof iterative circuits – ASM chart and realization of ASM chart, Timing issues in sequential circuits.

UNIT 2: DATAPATH AND CONTROLLER DESIGN **12 Hrs.**

Design and Synthesis of Datapath and Controller, Partitioned sequential machines, Design example: Design and synthesis of a RISC stored-program machine: ALU, Instruction Set Architecture, Controller Design and program Execution, UART design: Operation, Transmitter, Receiver.

UNIT 3: DESIGNING OF ARITHMETIC BUILDING BLOCKS **10 Hrs.**

Adder circuits: Carry Lookahead Adder, Conditional Sum Adder, Signed and Unsigned Array Multiplier, Booth Multiplier, Floating point adder, Propagation delay and critical path analysis, CORDIC algorithms and architectures, Distributed Arithmetic structure.

UNIT4: DESIGNING WITH FPGAS **10 Hrs.**

Introduction to FPGA architectures: Overview, programming technologies, Logic block architecture: FPGA logic cells, timing models, power dissipation, I/O block architecture: Input and Output cell characteristics, clock input, Timing, Power dissipation, Programmable interconnect - Partitioning and Placement, Routing resources, delays.

TOTAL HOURS: 42 Hrs.

COURSE OUTCOMES

On completion of the course, the student will be able to:

CO1 : Remember the concept of digital logic design.
CO2 : Understand the concept of datapath and controller modules of a digital system.
CO3 : Apply the knowledge to design and optimize the performance of a digital system.
CO4 : Analyse the performance parameters for a digital system.
CO5 : Evaluate different performance parameters and modify the circuits to achieve that.
CO6 : Design efficient digital systems with targeted performance parameter.

TEXT/REFERENCE BOOKS

1. Michael d. Ciletti, "advanced digital design with the verilog hdl, pearson education.
2. Stephen brown, zvonko vranesic, "fundamentals of digital logic with verilog", mcgraw-hill-2007.
3. Digital design: with an introduction to the verilog hdl, vhdl, and system verilog, 6e
4. Keshab k. Parhi, vlsi digital signal processing systems, wiley india pvt. Ltd, 2012
5. P K meher, arithmetic circuits for dsp applications, john wiley and sons ltd, 2017
6. Advanced fpga design: architecture, implementation, and optimization by steve kilts. Isbn: 9780470054376, publishers: wiley, 2007
7. Field-programmable gate arrays: reconfigurable logic for rapid prototyping and implementation of digital systems by richard c. Dorf, john v. Oldfield. Isbn: 9788126516612, publisher: wiley, 200

<Course Code>					IC Fabrication Technology					
Teaching Scheme					Examination Scheme					
L	T	P	C	Hrs./Week	Theory			Practical		Total Marks
					MS	ES	IA	LW	LE/Viva	
2	0	0	2	2	25	50	25	--	--	100

COURSE OBJECTIVES:

- To develop a comprehensive understanding of the fundamental processes and steps employed within the semiconductor industry, as well as the challenges it faces in keeping compliance with moore's law.
- To develop the fundamental understanding about mechanism and physics behind several processes and fabrication techniques being used during semiconductor devices and ic fabrication.
- To develop an understanding about back-end technology.

UNIT-1: INTRODUCTION, CRYSTAL GROWTH AND CLEANROOM **6 Hrs.**

Moore‟s Law, Scaling, Key semiconductor technologies; Crystal structure: Bravais lattice, Miller‟s Indices, and example; Crystal defects - Point defects, Linear defects, and volume defects; Raw materials and purification, Crystal growth - Czochralski and Float-Zone processes, CMP, Wafer specifications; Contamination Control: Cleanroom - features, classifications and guidelines; Wafer Cleaning, Gettering.

UNIT-2: DIFFUSION, AND ION-IMPLANTATION AND OXIDATION **8 Hrs.**

Doping process: Diffusion vs. ion-implantation, Diffusion - doping profile of PN-junction, Trends in diffusion, Solid solubility, Diffusion-coefficient, Fick‟s second law, Diffusion furnaces - Horizontal vs. vertical. Ion-implantation: History and significance, applications and advantage - disadvantages, Ion implantation process steps, Dose, energy, and angle considerations, Implantation damage and annealing - RTA, Channeling and shadowing effect. Oxidation: Dry vs wet oxidation, LOCOS, Thermal oxidation furnaces: Horizontal vs. vertical - their mechanism, Si/SiO2 interface, Oxide growth charges; growth kinetics, Deal-Grove model, Physical measurement: Ellipsometry, measurement by CV method.

UNIT-3: ETCHING AND LITHOGRAPHY **6 Hrs.**

Etching: Types - Wet and dry etch, an-isotropic and isotropic, Selectivity, Plasma etching and RIE; Photo-lithography: Introduction and its application to IC manufacturing, Light sources, Photo-mask, Wafer exposure system: contact proximity and projection printing, Immersion lithography, Resolution and depth of focus, Photo-resists: types, and issues; Process flow for lithography.

UNIT-4: THINFILM DEPOSITION AND BACK-END TECHNOLOGY **8 Hrs.**

Thin film deposition: requirements, typical steps, characteristics and step coverage, Chemical vapor deposition (CVD) techniques and their types; Physical vapor deposition (PVD) techniques: thermal and e-beam, Sputtering: Types - DC and RF sputtering, process parameters and applications; Atomic layer deposition (ALD); CMOS fabrication process flow. Back-end technology: Interconnects in CMOS technology, Advantages, Challenges posed, Interconnect fabrication process; Packaging assembly technology: Wafer thinning, Dicing, Die-attach, Wire-bond & Flip-chip process, Encapsulation, Laser marking, Solder ball attach, Singulation.

Max Hrs.: 28 Hrs.

COURSE OUTCOMES:

On completion of the course, student will be able to

CO1: understand the trends in semiconductor technology.
CO2: learn about cleanroom protocols, safety, gowning, and contamination control techniques.
CO3: to gain a comprehensive understanding of the various fabrication processes involved in semiconductor manufacturing such as etching, lithography, oxidation, diffusion, and ion implantation.
CO4: develop in-depth understanding of several thin film deposition techniques such as cvd, sputtering, evaporation, and ald.
CO5: assess the different fabrication steps and processes used in device manufacturing both in research and industrial contexts.
CO6: understand the fundamental processes involved in back-end technology.

TEXT/REFERENCE BOOKS:

1. J. D. Plummer, M. D. Deal & P. B. Griffin, Silicon Vlsi Technology, Prentice-Hall, 2000.
2. R.C. Jaeger, Introduction To Microelectronic Fabrication, Prentice Hall, Second Edition, 2013.
3. Chen, A., & Lo, R. H., Semiconductor Packaging: Materials Interaction And Reliability. Crc Press, 2016
4. Peer Reviewed Journal Papers/Conference Publications.

<Course Code>					Device Simulation Lab					
Teaching Scheme					Examination Scheme					
L	T	P	C	Hrs/Week	Theory			Practical		Total Marks
					MS	ES	IA	LW	LE/Viva	
0	0	2	1	2	--	--	--	50	50	100

COURSE OBJECTIVES

- To understand the characteristics and concepts related to the design of semiconductor devices.
- To explore different semiconductor devices and performance parameters at the device level.
- To analyse the performance of devices and use them for circuit applications.

LIST OF EXPERIMENTS

1 To study the simulation tool and its features for device simulation.

2 To design and implement diode for different doping profiles and analyze v-i characteristics, mobility, energy bands, Electric field and potential distribution.

3 To design and implement the mosfet with uniform and gaussian doping profile and analyze v-i characteristics, Mobility, energy bands, electric field and potential distribution.

4 To design and implement long channel mosfet with the channel length > 100 µm and analyze v-i characteristics, Mobility, energy bands, electric field and potential distribution.

5 To design and implement short channel mosfet with the channel length < 90 nm and analyze v-i characteristics, Mobility, energy bands, electric field and potential distribution.

6 To design and implement dgmosfet and analyze v-i characteristics, mobility, energy bands, electric field and Potential distribution.

7 To design inverter circuit with the help of implemented mosfet using mixed mode simulation and perform Transient and dc analysis.

8 To design and implement the inverter using cmos technology on the single semiconductor material.

COURSE OUTCOMES

On completion of the course, student will be able to:

CO1 : Identify the pros and cons, and the trends related to scaling of semiconductor device.
CO2 : Understand the characteristics, sub-parts, and the regions of operation of the mosfet and other devices.
CO3 : Design mosfet and other semiconductor devices for different doping profile and channel length.
CO4 : Estimate the performance of mosfet for different technology standard.
CO5 : Analyze and compare various device parameters for mosfet
CO6 : Create digital inverters with designed device using mixed mode simulation and cmos technology.

<Course Code>					Analog IC Design Lab					
Teaching Scheme					Examination Scheme					
L	T	P	C	Hrs/Week	Theory			Practical		Total Marks
					MS	ES	IA	LW	LE/Viva	
0	0	2	1	2	--	--	--	50	50	100

COURSE OBJECTIVES

1. To understand, analysis and design of mosfet-circuits, current mirrors, and feedback.
2. To understand, analysis and design of cmos operational amplifiers.
3. To understand, analysis and design of cmos oscillators.

LIST OF EXPERIMENTS

1 To study cadence tutorial, and design and analyze mos iv curves
2 To design and analyze cs with passive, active, and source degeneration
3 To design and analyze cg and cascode mosfet-circuits
4 To design and analyze current mirror and cascode mirror
5 To design and analyze differential amplifiers
6 To design and analyze feedback amplifiers
7 To design and analyze frequency response
8 To design and analyze operational amplifiers
9 To design and analyze oscillators
10 To design project

COURSE OUTCOMES

On completion of the course, student will be able to:

CO1 : Identify different mosfet-circuit configurations.
CO2 : Understand the current mirrors.
CO3 : Design the cmos feedback amplifier circuits.
CO4 : Analyze the design of the application-specific cmos operational amplifiers.
CO5 : Evaluate the robust and high-performance cmos oscillators.
CO6 : Create the design of advanced analog integrated circuits as per the application-specific requirements.

TEXT/REFERENCE BOOKS

1. Behzad razavi, “design of analog cmos integrated circuits,” 2nd edition, mcgraw hill, 2017.
2. J. Michael jacob, “applications and design with analog integrated circuits,” phi, 2nd edition, 2004.
3. Paul r. Gray, paul j. Hurst, stephen h. Lewis, robert g. Meyer, “analysis and design of analog integrated circuits,” 5th edition, wiley, 2009.
4. Sedra and smith, microelectronic circuits, oxford university press, 5th edition, 2005.

<Course Code>					Digital IC Design Lab					
TeachingScheme					Examination Scheme					
L	T	P	C	Hrs/Week	Theory			Practical		Total
					MS	ES	IA	LW	LE/Viva	
0	0	2	1	2	0	0	0	50	50	100

COURSE OBJECTIVES

- To learn how to create layout designs for CMOS circuits. This involves understanding the physical aspects of CMOS, like transistor placement, routing, and metal layers.
- To Use CAD (Computer-Aided Design) tools to simulate and verify the functionality of CMOS designs.
- To Gain proficiency in designing digital integrated circuits using CMOS technology. This includes understanding the basics of CMOS design, such as logic gates, flip-flops, and other digital building blocks.

Laboratory Sessions would be based on following topics:

1. To design layout of the CMOS INV and perform the RCX extraction and measure the delays.
2. To design layout of the CMOS NAND2 and perform the RCX extraction and measure the delays.
3. To design layout of the CMOS NOR2 and perform the RCX extraction and measure the delays.
4. To measure the dynamic and static power consumption of the CMOS NAND gate.
5. To understand the FO4 delay and measure the FO4 delay of the INV.
6. To apply the Logical effort technique to reduce the path delay.
7. To design layout of the Pass transistor AND2 and perform the RCX extraction and measure the delays.
8. To design layout of the DOMINO NAND2 and perform the RCX extraction and measure the delays.
9. To design layout of the Pseudo-NMOS NOR2 and perform the RCX extraction and measure the delays.
10. RTL to GDSII (Synthesis using digital gate library)
11. RTL to GDSII (Placement and Routing)
12. RTL to GDSII (CTC and STA)

COURSE OUTCOMES

On completion of the course, students will be able to:

CO1: Identify the pros and cons, and the trends related to VLSI Design.
CO2: Create layout designs for CMOS circuits and measure the performance metrics.
CO3: Understand the physical aspects of CMOS, including transistor placement, routing, and the use of metal layers.
CO4: Use CAD tools to simulate and verify the functionality of CMOS designs.
CO5: Perform static timing analysis to ensure that CMOS circuits meet their timing constraints.
CO6: Use techniques for minimizing power consumption in CMOS circuits. Understand the trade-offs between speed, power, and area.

TEXT/REFERENCE BOOKS

1. Neil Weste, David Harris, Ayan Banerjee, "CMOS VLSI design: A circuits and systems perspective", 3rd Edition, Pearson.
2. Sung-Mo Kang, Yusuf Leblebici , "CMOS Digital Integrated Circuits", 3rd Edition, Tata McGraw Hill.

<Course Code>					FPGA-based System Design Lab					
Teaching Scheme					Examination Scheme					
L	T	P	C	Hrs/Week	Theory			Practical		Total Marks
					MS	ES	IA	LW	LE/Viva	
0	0	2	1	2	--	--	--	50	50	100

COURSE OBJECTIVES

- To get an in-depth knowledge of hardware modelling using verilog hdl.
- To get an in-depth knowledge of digital system design using fpga.
- To analyses the different performance parameters (speed, power and area) of a digital system.

LIST OF EXPERIMENTS

1 Design and simulation of the combinational circuits using structural/dataflow Modelling and module instantiation technique. Report the resource utilization summery after implementation:
(a) 4-bit ripple carry adder (b) 4-bit adder-subtractor circuit.

2 Design and simulation of the combinational circuits using behavioral modelling (procedural Statements). Report the resource utilization summery after implementation:
(a) multiplexer (b) decoder (c) priority encoder (d) bcd to seven segment display decoder

3 Design and simulation of unsigned/signed array multipliers (use module instantiation technique). Report the resource utilization summery after implementation.

4 Design and simulation of the sequential circuits (explain blocking and non-blocking assignments). Report the resource utilization summery after implementation
(a) loadable up/down counters. (b) controllable left and right shift registers. (c) universal shift registers.

5 Memory design: design rom, ram and dual port memory using behavioral modelling and ip cores For 4- bit data width and 3-bit address.

6 Design and simulation of the following digital systems using fsm design style in behavioral hdl Modelling
(a) sequence detectors using mealy and moore machine.

7 Design and simulation of the pipelined and non-pipelined floating point adder. Report the resource Utilization and timing summery after each implementation.

8 ***Fpga based system design***
In this section, fixed point data representation will be used and data width will be chosen based on the design specifications. This experiment is divided into some objectives which are to be covered in 4-6 days.
I) design entry in verilog rtl modelling. Ii) synthesis and implementation using timing constraints.
III) Find maximum frequency and hardware resources. Iv) find dynamic power consumption.
IV) Implement the design in the fpga evaluation board and observe the output (s).
Here any of the two experiments will be performed
(A) Datapath and controller design (asm chart realization using verilog hdl): booth multiplier design
(B) Design of a basic processor: alu, datapath, controller and isa.
(C) Cordic architectures: vectoring and rotation mode.
(D) Fpga implementation of machine learning algorithms: implement a basic prototype of k-means clustering algorithm.

COURSE OUTCOMES

On completion of the course, student will be able to:

CO1 : Identify the construct of verilog hdl.
CO2 : Understand different modelling styles of verilog hdl.
CO3 : Apply the knowledge of verilog modelling to design digital systems.
CO4 Analyze the performance parameters of the digital systems.
CO5 : Evaluate the performance parameters based on the design constraints.
CO6 Design and implement a digital system based on the design constraints

TEXT/REFERENCE BOOKS

1. Michael d. Ciletti, "advanced digital design with the verilog hdl," pearson education.

<Course Code>					Scientific Writing and Publication Ethics					
Teaching Scheme					Examination Scheme					
L	T	P	C	Hrs./Week	Theory			Practical		Total Marks
					MS	ES	IA	LW	LE/Viva	
2	0	0	2	2	25	50	25	--	--	100

COURSE OBJECTIVES

1. To comprehend the significance of scientific writing and to understand of the basic structure of a scientific paper.
2. To get familiarize with the process of selecting appropriate target journals and conferences.
3. To cultivate an awareness of publication ethics within the realm of scientific writing.
4. To get acquainted with the knowledge and tools necessary to identify, understand, and avoid plagiarism in scientific writing

UNIT-1: INTRODUCTION TO SCIENTIFIC WRITING **07 Hrs.**

Importance of scientific writing in engineering, understanding the structure and components of a scientific paper, research paper writing style, referencing style

UNIT 2: SELECTING TARGET JOURNALS AND CONFERENCES **07 Hrs.**

Types of journals and conferences in engineering, open access journals, journal impact factors, conference rankings, manuscript submission process, responding to reviewer comments

UNIT 3: PUBLICATION ETHICS **07 Hrs.**

Introduction and importance, publication misconduct, violation of publication ethics, falsification and/or fabrication of data, understanding of copyright form, collaboration issues (authorship), conflicts of interest issues, Committee on Publication Ethics (COPE)

UNIT 4: AVOIDING PLAGIARISM **07 Hrs.**

Plagiarism – definition, reasons for plagiarism, types of plagiarism, avoiding plagiarism

TOTAL 28 Hrs

COURSE OUTCOMES

On completion of the course, students will be able to:

CO1 - Describe the importance of scientific writing in engineering and identifying its role in knowledge dissemination and academic integrity
CO2 - Understand the structure and components of a scientific paper
CO3 - **E**valuate and select suitable journals and conferences to submit their research work
CO4 - Understand publication ethics
CO5 - Define plagiarism, identify its different types and reasons, and apply techniques to avoid plagiarism
CO6 - Analyze and respond to reviewer comments for their research work

TEXT/REFERENCE BOOKS

1. Getting it published: a guide for scholars and anyone else serious about serious books by william germano
2. Publish and flourish: become a prolific scholar by tara gray
3. Adil e. Shamoo, and david b. Resnik, responsible conduct of research, oxford university press
4. Gary comstock, research ethics: a philosophical guide to the responsible conduct of research, cambridge university press
5. Tony mayer, and nicholas h. Steneck, promoting research integrity in a global environment, world scientific publishing
6. Ethical issues in engineering research, publication, and practice by caroline whitbeck

Semester 2

<Course Code>					Mixed-Signal VLSI Design					
Teaching Scheme					Examination Scheme					
L	T	P	C	Hrs./Week	Theory			Practical		Total Marks
					MS	ES	IA	LW	LE/Viva	
3	0	0	3	3	25	50	25	--	--	100

COURSE OBJECTIVES

- To learn the fundamentals of mixed-signal circuit design.
- To study of data converters (adc/dac) for interfacing of analog and digital systems.
- To know the various methods for the co-existence of analog and digital circuits on a single chip.

UNIT I: INTRODUCTION TO MIXED-SIGNAL **10 Hrs.**

Definition of Mixed-signal ICs, Challenges, Applications, Basic to data conversion and processing, Sampling, Switched capacitors circuits: MOSFET as switches, Diode as Switch, Switched Capacitor Integrator, MOS sample-hold circuits, Current mirror, Voltage-Controlled Oscillators (VCO), Phase Locked Loop (PLL), non- ideal effect in PLL, Jitter and phase noise and applications.

UNIT II: ANALOG-TO-DIGITAL CONVERTERS **12 Hrs.**

Performance Metric, Flash Architectures, Two-Step Architectures, Interpolative and Folding Architectures, Pipelined Architectures, Successive Approximation Architectures, Interleaved Architectures, Over sampling ADC – Noise shaping, Sigma-Delta modulator.

UNIT III: DIGITAL-TO-ANALOG CONVERTERS **10 Hrs.**

Performance Metrics, Reference Multiplication and Division: Voltage Division, Current Division, Charge Division, Switching and logical Functions in DACs, Switching Functions in Resistor-Ladder DACs, Switching Functions in Current-Steering DACs, Switching Functions in Capacitor DACs, Binary-to-Thermometer Code Conversion,

Architectures: Resistor-Ladder DAC Architectures, Ladder Architecture with Switched Sub-divider, Intermeshed Ladder Architectures, Current-Steering Architectures, R-2R-Network Based Architectures, Segmented Architectures

UNIT IV: NOISE AND TESTING OF ICs **10 Hrs.**

Noise: Types of noise: Shot, Thermal, Flicker (1/f), Burst, and avalanche noise, Noise Models of IC components: Diode, BJT, MOS transistor, Resistor, capacitors, and inductors, Noise power trade-off, Noise Bandwidth, Noise Figure, Noise Temperature, Total harmonic distortion.

Testing: General Consideration, Sampling circuits, D/A converters, A/D convertors: static and dynamic testing.

Project

TOTAL HOURS: 42 Hrs.

COURSE OUTCOMES

On completion of the course, student will be able to:

CO1 : Define the importance of mixed-signal circuits in ic design.
CO2 : Understand the principles and mathematical concepts of different mixed-signal circuit architectures.
CO3 : Apply the appropriate amplifier circuit to amplify analog and discrete signals.
CO4 : Analyze and compare the performance metrics of data converters.
CO5 : Evaluate the various a/d and d/a converters for a given data acquisition system.
CO6 : Design the mixed-signal circuit ic for real-life applications.

TEXT/REFERENCE BOOKS

1. Behzad razavi, “design of analog cmos integrated circuits,” mcgraw-hill international edition 2016.
2. Behzad razavi, “principles of data conversion system design,” wiley-ieee press, 1995
3. R. Jacob baker, “cmos mixed-signal circuit design,” wiley india, ieee press, and reprint 2008.
4. Tony chan carusone, david a. Johns, kenneth w. Martin, “analog integrated circuit design,” wiley, 2nd edition.

<Course Code>					Mixed-Signal VLSI Design Lab					
Teaching Scheme					Examination Scheme					
L	T	P	C	Hrs/Week	Theory			Practical		Total Marks
					MS	ES	IA	LW	LE/Viva	
0	0	2	1	2	--	--	--	50	50	100

COURSE OBJECTIVES

1. To understand analysis and design of analog-to-digital converters.
2. To understand analysis and design of digital-to-analog-converters.
3. To understand analysis and design of co-existence of analog and digital circuits on a single chip.

LIST OF EXPERIMENTS

1 Introduction to circuit design and device simulation tools.
2 To design switched-capacitor and sample and hold circuits.
3 To design current mirror circuits
4 To design comparator circuits
5 To design integrator circuits
6 To design voltage-controlled oscillator circuit.
7 To design phase locked loop circuit.
8 To design analog-to-digital converters.
9 To design digital-to-analog-converters.
10 Project

COURSE OUTCOMES

On completion of the course, student will be able to:

CO1 : Understand and apply the principles and mathematical concepts of different mixed-signal circuit architectures.
CO2 : Design the application-specific amplifier circuit to amplify analog and digital signals.
CO3 : Design and compare the performance metrics of data converters.
CO4 : Evaluate the various a/d and d/a converters for a given data acquisition system.
CO5 : Design the mixed-signal circuits in ic design.
CO6 : Create the design of the mixed-signal circuit ic for real-life applications.

TEXT/REFERENCE BOOKS

1. Behzad razavi, “design of analog cmos integrated circuits,” mcgraw-hill international edition 2016.
2. Behzad razavi, “principles of data conversion system design,” wiley-ieee press, 1995
3. R. Jacob baker, “cmos mixed-signal circuit design,” wiley india, ieee press, and reprint 2008.
4. Tony chan carusone, david a. Johns, kenneth w. Martin, “analog integrated circuit design,” wiley, 2nd edition.

<Course Code>					Research Methodology					
Teaching Scheme					Examination Scheme					
L	T	P	C	Hrs./Week	Theory			Practical		Total Marks
					MS	ES	IA	LW	LE/Viva	
2	0	0	2	2	25	50	25	--	--	100

COURSE OBJECTIVES

1. To understand the role of research in the field of engineering and get an overview of the research process.
2. To develop proficiency in literature review techniques.
3. To understand the process of formulating and solving research problems.
4. To understand different types of intellectual property rights.

UNIT I : INTRODUCTION TO RESEARCH **06 Hrs.**

Role of research in engineering, research process overview, types of research, outcomes of research, characteristics of a researcher, research terminology

UNIT II : LITERATURE REVIEW TECHNIQUES **06 Hrs.**

Searching for the existing literature, reviewing the selected literature, developing a theoretical framework, developing a conceptual framework

UNIT III : FORMULATING AND SOLVING A RESEARCH PROBLEM **08 Hrs.**

Importance of formulating a research problem, sources of research problems, identifying a problem, formulation of research objectives and research questions, Need for research design, different research designs, experimental test-setups, data sampling, data collection, data analysis & interpretation

UNIT VI: INTELLECTUAL PROPERTY RIGHTS **08 Hrs.**

Introduction and significance of intellectual property rights, types of intellectual property rights, introduction to patents, patent drafting and filing, copyright, trademarks, industrial design, geographical indicators

Total: 28 Hrs.

COURSE OUTCOMES

On completion of the course, student will be able to:

CO1 - Understand the role and significance of research in engineering
CO2 - Develop understanding of the basic framework of research process and design
CO3 - Identify technical gaps in the literature and formulate a problem.
CO4 - Develop an understanding of various research designs and techniques.
CO5 - Develop an understanding of the ethical dimensions of conducting applied research
CO6 - Evaluate and apply intellectual property rights concepts to the research outcomes

TEXT/REFERENCE BOOKS

1. Stuart melville, wayne goddard, research methodology: an introduction for science and engineering students, juta & co. Ltd.
2. David v. Thiel, research methods for engineers, cambridge university press, uk
3. Ranjit kumar, research methodology: a step by step guide for beginners, pearson
4. Cr kothari, research methodology (methods and techniques), new age publications

Core Elective (with Lab)

Professional Core Elective_L-1

<Course Code>					Testing and Verification of VLSI Circuits					
TeachingScheme					Examination Scheme					
L	T	P	C	Hrs/Week	Theory			Practical		Total
					MS	ES	IA	LW	LE/Viva	
3	0	0	3	3	25	50	25	--	--	100

COURSE OBJECTIVES

- To understand the concepts of testing and verification in VLSI circuits.
- To understand the methodology used to ensure reliability of integrated circuits.
- To understand various verification methodologies.

UNIT-1: Introduction to Testing **(6 Hrs)**

Scope of Testing and Verification in VLSI Design Process, Issues in Test and Verification of complex chips, embedded cores and SoCs, Fundamentals of VLSI Testing, Fault Modelling, Logic Simulation andFault Simulation, Deductive Fault Simulation Algorithms, Automatic Test Pattern Generation

UNIT-2: Design for Testability **(8 Hrs)**

Design for testability, Scan design, Test interface and boundary scan, System testing and test for SOCs, Built-in Self Test (BIST) – Exhaustive Pattern Generation, Random Pattern Generation, BIST for testing of logic andmemories, fault detection by MARCH tests Issues in test, Test automation

UNIT-3: Verification Methodologies **(6 Hrs)**

Design verification techniques based on simulation, analytical and formal approaches. Functional verification. Timing verification. Formal verification. Basics of equivalence checking and model checking. Hardware emulation.

UNIT-4: System Verilog for Verification **(8 Hrs)**

Introduction to System Verilog – Literal values-data Types – Arrays – Array methods – Creating new types with typedef – user defined structures – Enumerated types – attributes - operators – expressions -Procedural statements and control flow

- Processes in System Verilog – Task and functions – Routine arguments – Returning from a routine, Program, Interface, Stimulus timing, Module interactions, Test Bench

Max. 28Hrs.

COURSE OUTCOMES

On completion of the course, the student will be able to:

CO1: Generateeffective testpatternsautomatically for variousfault models. CO2:
Design VLSI circuits with built-in testability features.
CO3: Apply fault simulation techniques to identify the potential issues
CO4: Perform formal and simulation-based verification to ensure correctness of design
CO5: Perform static timing analysis to validate the circuits
CO6: Apply testing and verification techniques to identify and resolve issues in real world VLSI design

TEXT/REFERENCE BOOKS

1. M. L. Bushnell and V.D. Agrawal, Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits, Springer, 2005
2. M. Abramovici, M. Breuer, and A. Friedman, Digital System Testing and Testable Design, IEEE Press, 1994
3. H. Fujiwara, Logic Testing and Design for Testability, MIT Press, 1985
4. Vanessa R. Copper, "Getting started with UVM: A Beginner"s Guide", Verilab Publishing, First Edition, 2013
5. Ray Salmei, "The UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology" Boston Light Press; First edition, 2013
6. Christian B Spear, "System Verilog for Verification: A guide to learning the Testbench language features",Springer publications, Third Edition, 2012

Professional Core Elective_P-1

<Course Code>					Testing and Verification of VLSI Circuits Lab					
Teaching Scheme					Examination Scheme					
L	T	P	C	Hrs/Week	Theory			Practical		Total
					MS	ES	IA	LW	LE/Viva	
0	0	2	1	2	--	--	--	50	50	100

COURSE OBJECTIVES

- To understand system Verilog RTL design and synthesis features for verification
- To Understand the concept of verification plan for real time implementation
- To apply the system Verilog verification features for more effective and efficient verification.

List of Experiments:

1. To Understand the role of system verilog for verification
2. Program to realize standard data types, literals, procedure statements and procedural blocks
3. Program to understand operators, static Arrays, User defined Data type and structures
4. Program to understand static Arrays, Hierarchy and connectivity
5. Program to understand Queues and Dynamic and Associative Arrays (QDA)
6. Implement Clocking Blocks to perform verification
7. Implement Interprocesssynchronizationandinterfaces for verification
8. Program to understand polymorphism and virtuality for verification
9. Introduction to assertion-based Verification (ABV)
10. Introduction to system verilog assertions (SVA)
11. Introduction to Device Under Test (DUT)

COURSE OUTCOMES

On completion of the course, the student will be able to:
CO1: Understand the basic concepts of system verilog including data types, operators, and control structures CO2: Understand the concepts of verification methodologies
CO3: The ability to identify and debug issues in system verilog designs and test benches CO4: To understand the synthesis process and ability to optimize the code
CO5: Analyze the concepts of functional coverage
CO6: Understanding assertions for design verification and formal methods for design correctness.

TEXT/REFERENCE BOOKS

1. Spear, Chris, Tumbush, Greg. System Verilog for Verification, 2nd Edition, Springer, 2008
2. Vijayaraghavan, Srikanth, and Meyyappan Ramanathan. A practical guide for System Verilog assertions, Springer Science & Business Media, 2006
3. Bergeron, Janick. Writing testbenches using System Verilog, 1st Edition, Springer Science & Business Media, 2007

Professional Core Elective_L –2

<Course Code>					VLSI Physical Design					
Teaching Scheme					Examination Scheme					
					Theory			Practical		Tot
L	T	P	C	Hrs/Week	MS	ES	IA	LW	LE/Viva	al
3	0	0	3	3	25	50	25	--	--	100

COURSE OBJECTIVES:

- To develop understanding of state-of-the-art tools and algorithms that address floor planning design tasks.
- To develop understanding of state-of-the-art tools and algorithms that address module placement and routing design tasks.
- To develop understanding of signal routing for vlsi logic and physical level design.

UNIT-1: INTRODUCTION **5 Hrs.**

Layout and design rules, materials for VLSI fabrication, basic algorithmic concepts for physical design, physical design processes and complexities.

UNIT-2: PARTITION AND FLOOR PLANNING **8 Hrs.**

Partition: Kernigham-Lin‟s algorithm, Fiduccia Mattheyes algorithm, Krishnamurty extension, hMETIS algorithm, multilevel partition techniques.

Floor-Planning: Hierarchical design, wirelength estimation, slicing and non- slicing floor plan, polar graph representation, operator concept, Stockmeyer algorithm for floor planning, mixed integer linear program.

UNIT-3: PLACEMENT AND ROUTING **9 Hrs.**

Placement: Design types: ASICs, SoC, microprocessor RLM; Placement Techniques: Simulated annealing, partition-based, analytical, and Hall‟s quadratic; Timing and congestion considerations.

Routing: Detailed, global and specialized routing, channel ordering, channel Routing problems and constraint graphs, routing algorithms, Yoshimura and Kuh‟s method, zone scanning and net merging, boundary terminal problem, minimum density spanning forest problem, topological routing, cluster graph representation.

UNIT-4: SEQUENTIAL LOGIC OPTIMIZATION AND CELL BINDING **06 Hrs.**

State based optimization, state minimization, algorithms; Library binding and its algorithms, concurrent binding

Max Hrs. 28

COURSE OUTCOMES:

On completion of the course, the student will be able to:

CO1 – Understand different types of vlsi design flows.
CO2 – Synthesize the given design by considering various constraints and to optimize the same.
CO3 – Understand various timing parameters and compute computation time for a given design using timing analysis.
CO4 – Perform physical design by adhering to guidelines.
CO5 – Apprehend the importance of physical design verification
CO6 – Design vlsi systems using industry standard tools.

TEXT/REFERENCE BOOKS:

1. M. Sarrafzadeh, and c. K. Wong, an introduction to vlsi physical design, 4th ed., mcgraw-hill, 1996.
2. W. Wolf, modern vlsi design system on silicon, 2nd ed., pearson education, 2000.
3. S. M. Sait, and h. Youssef, vlsi physical design automation: theory and practice, world scientific, 1999.
4. R. Dreschler, evolutionary algorithms for vlsi cad, 3rd ed., springer, 2002.
5. N. A. Sherwani, algorithm for vlsi physical design automation, 2nd ed., kluwer, 1999.
6. S. K. Lim, practical problems in vlsi physical design automation, springer, 2008.

<Course Code>					VLSI Physical Design Lab					
TeachingScheme					Examination Scheme					
L	T	P	C	Hrs/Week	Theory			Practical		Total
					MS	ES	IA	LW	LE/Viva	
0	0	2	1	2	--	--	--	50	50	100

COURSE OBJECTIVES

- To understand how to design digital circuits at the rtl level using hardware description languages (hdls) like vhdl or verilog, which involves writing and verifying rtl code.
- To provide students or participants with practical, hands-on experience in the complete ic design flow from rtl description to physical layout.
- To help participants understand the various stages of the ic design flow, including synthesis, physical design, and verification.

Laboratory Sessions would be based on following topics:

Laboratory sessions cover the practical on various steps of RTL to GDSII design flow on Cadence.

1. Code a design in verilog to the design specification that is provided. Write a verilog code for combinational and sequential circuits.
2. Write a testbench to perform the functional verification of the design.
3. Write a tcl script to automate the process of synthesis, and elaborate design to get the timing, power, andarea information.
4. Importing a synthesized design in innovus and preparing floor planning and placement of the synthesis design.
5. Perform the clock tree synthesis and routing.
6. Perform the static timing analysis to detect timing violations (min-max delay analysis).
7. Identify the pin locations, add the i/o pads, and perform the post layout simulations.
8. Prepare a gds-ii of the alu using the steps discussed earlier.

COURSE OUTCOMES

On completion of the course, students will be able to

CO1: comprehend the entire integrated circuit (ic) design flow, from rtl description to gdsii tapeout. This includes the various steps involved in the design process.

CO2: design digital logic circuits at the rtl level using hardware description languages like vhdl or verilog.

CO3: use synthesis tools to convert rtl descriptions into gate-level netlists and perform optimizations for area, power, and timing.

CO4: understand the principles of design for testability (dft) and how to insert test structures like scan chains for easy manufacturing testing.

CO5: perform static timing analysis to ensure that circuits meet their timing constraints.

CO6: understand the process of preparing a design for tapeout, including generating gdsii files and creating documentation.

TEXT/REFERENCE BOOKS

1. Sneh saurabh, "introduction to vlsi design flow", cambridge university press, 2023
2. M.j.s. smith, "application-specificintegrated circuits", addison-wesley, 1997
3. L. Lavagno, i. L. Markov, g. Martin, and l. K. Scheffer (editors), "electronic design automation for ic implementation, circuit design, and process technology", crc press, 2016

Core Elective (without Lab)

<Course Code>					IC Manufacturing Packaging & Testing					
TeachingScheme					Examination Scheme					
L	T	P	C	Hrs/Week	Theory			Practical		Total
					MS	ES	IA	LW	LE/Viva	
3	0	0	3	3	25	50	25	--	--	100

COURSE OBJECTIVES

- To develop a comprehensive understanding of the fundamental processes and steps employed for ic package manufacturing within semiconductor industry.
- To develop an understanding of semiconductor component and package testing, including an exploration of challenges that contribute to their failures.
- To gain insights into the materials for industrial packaging, various reliability testing and the principles of quality and statistical control in the industry.

UNIT 1: SEMICONDUCTOR PACKAGE MANUFACTURING **10 Hrs**.

Packaging assembly technology: Wafer thinning, Dicing, Die-attach, Wire-bond & Flip chip process flow, Encapsulation, Laser Marking, Solder ball attach, Reflow, Flux cleaning, Underfill study, Singulation. IC packaging toolsets & equipment operation. Cleanroom operations.

UNIT 2: SEMICONDUCTOR COMPONENT AND PACKAGE TEST, AND FAILURE ANALYSIS **12 Hrs.** Setup and operation of test equipment, Wafer level burn-in & component testing process flow, Test programs development & debugging. In-line parametric testing, Wafer probe & final parametric testing. Functional testing at high and low temperature, Post electrical flow. Failure analysis: Package failure modes, Failure detection mechanisms, Failure analysis tools, Test programs debugging, Data analytics, ESD & EMI management.

UNIT 3: SEMICONDUCTOR PACKAGE MATERIALS AND QUALIFICATION **10 Hrs.**

Reliability testing & qualification – MST/MSL, TC/TS, HAST, HTSL, Lead Integrity, Solderability, Board level test. Mold compounds (Moldability), Underfill, Die attach adhesive, Substrate, Bonding wire, Solder & dielectric materials.

UNIT 4: INDUSTRIAL QUALITY AND STATISTICAL PROCESS CONTROL **10 Hrs**.

Quality Control Plan (QCP) & Quality Management System (QMS). Incoming inspection/In-line quality/MSA. SPC (Statistical Process Control) & Statistical analysis methods, FDC (Fault Detection Classification), Run-to-Run (R2R) control, Auto Defect Classification (ADC). Data analytics, machine communication protocol & system integration.

Max. 42 Hrs.

COURSE OUTCOMES

On completion of the course, student will be able to

CO1: Understand and learn the fundamental processes used for ic package manufacturing.

CO2: Explore diverse testing procedures employed for semiconductor components and packages.

CO3: Gain a comprehensive understanding of the package failure - modes, detection mechanisms and analysis tools.

CO4: Develop in-depth understanding of reliability testing & qualification applied to ic packages.

CO5: Understand and implement quality control, quality assurance and statistical procedures in semiconductor industry.

CO6: Develop in-depth knowledge about cleanroom operations.

TEXT/REFERENCE BOOKS

1. Rao R. Tummala – Fundamentals of Microsystems Packaging, McGraw Hill, NY, 2001
2. Rao R Tummala and Madhavan Swaminathan – Introduction to System-on-Package, McGraw Hill, 2008
3. R S Khandpur – Printed Circuit Boards, McGraw Hill, 2006.
4. Plummer, M. Deal and P. Griffin – Silicon VLSI Technology, Prentice Hall, 2001.
5. Peer reviewed Journal Papers/Conference publications.

<Course Code>					Low Power VLSI Design					
Teaching Scheme					Examination Scheme					
L	T	P	C	Hrs./Week	Theory			Practical		Total Marks
					MS	ES	IA	LW	LE/Viva	
3	0	0	3	3	25	50	25	--	--	100

COURSE OBJECTIVES:

COURSE OBJECTIVES

- Understand the concepts and techniques of low power vlsi.
- Develop a broad insight into the methods used to confront the low power issue from lower level (circuit level) to higher levels (system level) of abstraction.
- Develop a system with multiple supply and threshold voltages used for low power vlsi applications.

UNIT I: BASICS OF MOS CIRCUITS AND SOURCES OF POWER DISSIPATION **09 Hrs.**

MOS Transistor structure and device modeling, MOS Inverters, MOS Combinational Circuits - Different Logic Families, Dynamic Power Dissipation: Short Circuit Power, Switching Power, Glitching Power; Static Power Dissipation, Degrees of Freedom

UNIT II: SUPPLY VOLTAGE SCALING APPROACHES **11 Hrs.**

Device feature size scaling, Multi-Vdd Circuits, Architectural level approaches: Parallelism, Pipelining, Voltage scaling using high-level transformations, Dynamic voltage scaling, Power Management.

UNIT III: SWITCHED CAPACITANCE MINIMIZATION APPROACHES **11 Hrs.**

Formation of Partial Differential Equations (PDEs), Solutions of PDEs of first order, Cauchy problem for first order PDEs, Lagrange‟s method, Charpit and Jacobi methods for solving first order nonlinear PDEs.

UNIT IV: LEAKAGE POWER MINIMIZATION APPROACHES **11 Hrs.**

Variable-threshold-voltage CMOS (VTCMOS) approach, Multi-threshold-voltage CMOS (MTCMOS) approach, Power gating, Transistor stacking, Dual-Vt assignment approach (DTCMOS); Special Topics: Adiabatic Switching Circuits, Battery-aware Synthesis, Variation tolerant design, CAD tools for low power synthesis.

TOTAL HOURS: 42 Hrs.

COURSE OUTCOMES

On completion of the course, student will be able to:

CO1 : Identify the factors affecting the power in vlsi circuits.
CO2 : Understand the logic and circuit level power optimization techniques.
CO3 : Apply the low-power vlsi circuits based on the switched capacitance minimization approaches.
CO4 : Apply the low-power vlsi circuits based on the leakage power minimization approaches.
CO5 : Design and develop power efficient ips.
CO6 : Create, analyze, and design the advance low-power vlsi circuits.

TEXT/REFERENCE BOOKS

1. Sung mo kang, yusuf leblebici, “cmos digital integrated circuits,” tata mcgrag hill.
2. Neil h. E. Weste and k. Eshraghian, “principles of cmos vlsi design,” 2nd edition, addison wesley (indian reprint).
3. A. Bellamour, and m. I. Elmasri, “low power vlsi cmos circuit design,” kluwer academic press, 1995.
4. Anantha p. Chandrakasan and robert w. Brodersen, “low power digital cmos design,” kluwer academic publishers, 1995.
5. Kaushik roy and sharat c. Prasad, “low-power cmos vlsi design,” wiley-interscience, 2000.
6. A. Pal , “low power vlsi circuits and systems,” springer, india, 1st ed., 2014.

<Course Code>					VLSI Signal Processing Architecture					
Teaching Scheme					Examination Scheme					
					Theory			Practical		Tot
L	T	P	C	Hrs/Week	MS	ES	IA	LW	LE/Viva	al
3	0	0	3	3	25	50	25	--	--	100

COURSE OBJECTIVES:

- To learn architectures of signal processing algorithms for VLSI implementation
- To learn the design techniques to meet the performance goal (speed, power, and area)
- To learn the algorithm architecture co-design techniques for implementing efficient DSP systems

UNIT-1: Introduction to DSP systems **10 Hrs.**

VLSI design issues for signal processing and communication algorithms. Graphical representation of DSP algorithms, signal flow graph, data flow graph (DFG) and dependence graph (DG), concept of critical path. Iteration Bound: Definition, Examples, Algorithms for computing Iteration bound.

UNIT-2: Pipelining and parallel processing **11 Hrs.**

Retiming, cutset retiming, critical path minimization. Parallel realization by unfolding a DFG, properties of unfolding, retiming for unfolding, bit serial to digit serial and word serial conversions. Area minimization by folding, retiming for folding, folding for delay optimization.

UNIT-3: Systolic Array Architectures **11 Hrs.**

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Matrix Multiplication and 2D Systolic Array Design, Fast Convolution: Introduction, Cook, Toom Algorithm, Winogard Algorithm

UNIT-4: Arithmetic Architectures **10 Hrs.**

Bit level arithmetic structures, efficient multiplier architectures, Booth recoding, CSD, bit serial digital filters, multiplierless realization by distributed arithmetic, redundant arithmetic, CORDIC algorithm and Architectures.

Max Hrs. 42

COURSE OUTCOMES:

On completion of the course, the student will be able to:

CO1 – Identify various techniques to improve performance goal of the architecture.
CO2 – Understand the basics of VLSI DSP system design techniques.
CO3 – Apply the techniques to design an efficient VLSI system.
CO4 – Analyze the advantages and disadvantages of various techniques. CO5 – Evaluate the performance goal of the design
CO6 – Design a high-performance VLSI DSP system for real time applications.

TEXT/REFERENCE BOOKS:

1. Keshab K. Parhi, *VLSI Digital Signal Processing Systems*, Wiley India Pvt. Ltd, 2012
2. P K Meher, *Arithmetic Circuits for DSP Applications*, John Wiley and Sons Ltd, 2017

<Course Code>					RFIC Design					
TeachingScheme					Examination Scheme					
L	T	P	C	Hrs/Week	Theory			Practical		Total
					MS	ES	IA	LW	LE/Viva	
3	0	0	0	3	25	50	25	--	--	100

COURSE OBJECTIVES

- To learn the basic concepts of RF Design for modern radio transceivers
- To analyse the behaviour of high frequency components.
- To give understanding of design of various RF building-blocks

UNIT 1 Basic Concepts in RF Design **10 Hrs**

Effects of nonlinearity, gain compression, desensitization and blocking, intermodulation, IIP2, IIP3, cascaded nonlinear stages, intersymbol interference, noise figure, noise figure of cascaded stages, link budget analysis, sensitivity and dynamic range, passive impedance transformation. S-Parameters

UNIT 2: Transceiver Architecture **11 Hrs**

General considerations, heterodyne receiver, problem of image, direct conversion receiver, issues with DCR, low IF receiver, image reject receiver, digital IF receiver, Transmitter architectures: baseband/RF interface, PA/Antenna interface, direct conversion transmitters, transmitters performance tests. Mobile RF Communication systems and basics of Multiple Access techniques. Receiver system design, Modern transceiver case studies.

UNIT 3: Design and Integration of Passive Components **10 Hrs**

Characteristics of passive IC components at RF frequencies, interconnects, resistors, capacitors, inductors and transformers – Transmission lines. Generalization basic resonator and filter configurations: low pass, high pass, band pass and band stop type filters-filter implementation, on chip filters, on chip antennas.

UNIT 4: RF Sub System Design **11 Hrs**

Low-noise amplifiers: General considerations, problem of input Matching, LNA topologies, gain switching, band switching, high-IP2 LNAs and nonlinearity calculations. Mixers: passive down conversion mixers, active down conversion mixers, improved mixer topologies and up conversion mixers. Oscillators: basic principles, cross-coupled VCO, Phase Noise.

Max. 42 Hrs

COURSE OUTCOMES

On completion of the course, student will be able to

CO1: Understand the basics of RF system design

CO2: Define basic RF measurements parameters

CO3: Apply concepts of RF to modern transceivers.

CO4: Analyze performance measures for various receiver architectures.

CO5: Evaluate and compare performance of RF sub systems

CO6: Design RF sub systems

TEXT/REFERENCE BOOKS

1. Behzad Razavi, "RF Microelectronics" Prentice Hall of India (2001).
2. Bosco Leung, "VLSI for Wireless Communication", Springer (2011).
3. Razavi, B., "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill (2008).
4. D.M. Pozar, "Microwave Engineering", John Wiley
5. Thomas H. Lee, "The Design of CMOS Radio Frequency Integrated Circuits", Cambridge University Press.

<Course Code>					Advanced VLSI Interconnects					
Teaching Scheme					Examination Scheme					
L	T	P	C	Hrs./Week	Theory			Practical		Total Marks
					MS	ES	IA	LW	LE/Viva	
3	0	0	3	3	25	50	25	--	--	100

COURSE OBJECTIVES

- To understand analysis and design of conventional vlsi interconnects.
- To understand parasitic extraction, vlsi interconnects modeling and crosstalk analysis.
- To understand analysis and design of gnr-based and cnt-based vlsi interconnects.

UNIT I: INTRODUCTION TO VLSI INTERCONNECTS **10 Hrs.**

Interconnects for VLSI applications, metallic and optical interconnects, advantages of conventional copper (Cu) interconnects, challenges posed by Cu interconnects, fabrication process, even and odd mode capacitances, Miller theorem, transmission line equations, resistive interconnection as ladder network, propagation delays.

UNIT II: PARASITIC EXTRACTION IN VLSI INTERCONNECTS **12 Hrs.**

Parasitic resistance, effect of surface/interface scattering and diffusion barrier on resistance, Types of Capacitance: parallel-plate, fringing, and coupling capacitances, methods of capacitance extraction, Types of Inductance: self and mutual inductance, methods of inductance extraction, high-f losses, frequency-dependent parasitics, skin effect.

UNIT III: MODELING OF INTERCONNECTS AND CROSSTALK ANALYSIS **10 Hrs.**

Elmore model, Transfer function model, even and odd mode model, Time-domain analysis of multiconductor lines, transmission line interconnect models, Finite-Difference Time-Domain (FDTD) method, performance analysis of interconnect lines using linear (resistive) and non-linear (CMOS) drivers, advanced interconnect techniques to avoid crosstalk.

UNIT IV: GRAPHENE NANORIBBON AND CARBON NANOTUBE VLSI INTERCONNECTS **10 Hrs.**

Quantum electrical properties: quantum conductance, quantum capacitance, kinetic inductance, electron scattering and lattice vibrations, electron mean free path, Graphene nanoribbon (GNR) interconnects, single layer and multi-layer GNR resistance models, Carbon nanotube (CNT) interconnects, single-wall and multiwalled CNT resistance models, performance comparison of GNRs, CNTs and conventional interconnects.

TOTAL HOURS: 42 Hrs.

COURSE OUTCOMES

On completion of the course, student will be able to:

CO1 : Identify the crosstalk and delay in conventional vlsi interconnects.
CO2 : Understand the signal integrity analysis in gnr-based vlsi interconnects.
CO3 : Apply the signal integrity analysis in cnt-based vlsi interconnects
CO4 : Analyze and implement the fdtd model in conventional and novel vlsi interconnects
CO5 : Evaluate the designs and models of the advanced vlsi interconnects.
CO6 : Create the design of advanced vlsi interconnects models for the industry standard spice simulators.

TEXT/REFERENCE BOOKS

1. Ashok k. Goel, “high-speed vlsi interconnects,” 2nd edition, wiley, 2015.
2. Y. S. Diamand, t. Osaka, m. Datta, t. Ohba, “advanced nanoscale ulsi interconnects: fundamentals and applications,” springer, 2009.
3. H.-s. P. Wong, d. Akinwande, “carbon nanotube and graphene device physics,” cambridge university press, 2011.

<Course Code>					Mechatronics& Control for Semiconductor Manufacturing					
Teaching Scheme					Examination Scheme					
L	T	P	C	Hrs/Week	Theory			Practical		Total Marks
					MS	ES	IA	LW	LE/Viva	
3	0	0	3	3	25	50	25	--	--	100

COURSE OBJECTIVES

- To Understand the fundamental principles of mechatronics and control systems and their applications in the semiconductor manufacturing industry, gaining insight into the interdisciplinary nature of this field.
- Develop proficiency in analyzing, designing, and implementing control methods for mechatronic and robotic systems, specific to semiconductor manufacturing processes, with a focus on precision, repeatability, and quality control
- Acquire practical skills in using simulation tools, such as MATLAB/Simulink and Python, to design, optimize, and evaluate control systems for motion and manufacturing processes in semiconductor manufacturing, while addressing challenges related to uncertainties, nonlinearities, and disturbances in the manufacturing environment.

Unit 1: Introduction to Semiconductor Manufacturing 10Hrs

Review of Semiconductor Industry, Potential and Challenges in Semiconductor manufacturing, Manufacturing: An Interdisciplinary Science, Role of Mechatronics, Introduction to Semiconductor Manufacturing Processes with typical wafer processing overview, Introduction to techniques like PVD, CVD, RTP, CMP, Lithography, Clean room Technology and environmental control, Safety and quality control in semiconductor manufacturing

Unit 2: Mechatronics and Instrumentation in Semiconductor Manufacturing 10 Hrs.

Mechatronics in high-tech industries, Control and Instrumentation in Semiconductor Manufacturing, Applied physics in Mechatronic systems, Sensors and actuators in semiconductor manufacturing, Measurements and control, Precision and accuracy, Robotic solutions for semiconductor manufacturing, Types of robots and principles, Robotic arms, Mobile robots, Case studies on mechatronics and robots with Research trends.

Unit 3: Dynamics of Motion Systems and Analysis tools in Semiconductor Manufacturing 11 Hrs

Review of Feedback control Systems, Closed loop Transfer function and Disturbance rejection, Equilibrium and Stability notions, Degrees of Freedom and Configuration Space, Cause and response in static and dynamic systems, Various dynamical systems with examples, Dynamical equations of motion control Systems, State-space models of various practical systems, Solving system equations, Energy based modelling, Nonlinear Systems, Qualitative analysis, Linearization, Local behaviour of nonlinear systems, Feedback Linearization, Various stability analysis and methods.

Unit 4: Control Design with Simulation tools for Motion systems in Semiconductor Manufacturing 11 Hrs

Review of PID control, State feedback vs Output feedback, Pole placement, Various uncertainties in manufacturing processes: Parametric, approximated nonlinearities, disturbances, Types of robust controllers: Robust PID, Control Lyapunov method, SMC control, Optimization and Optimal Control, State estimation techniques, Machine learning based control, Simulations of various control in MATLAB/Simulink and Python. Research problems on the interface of Control and semiconductor manufacturing.

COURSE OUTCOMES: **Max. Hrs. 42**

After the completion of the course, students will be able to,

CO1. Identify various foundational concepts and processes involved in semiconductor manufacturing.
CO2. Understand the elements of mechatronic systems solutions in semiconductor manufacturing.
CO3. Understand the elements of instrumentation and robotic solutions in semiconductor manufacturing.
CO4. Apply various concepts of dynamics of motion systems with required physics for semiconductor manufacturing
CO5. Analyze systems and control tools used in semiconductor manufacturing systems using modern control tools.
CO6. Create and Evaluate different types of mechatronic and control solutions in semiconductor manufacturing.

TEXT/REFERENCE BOOKS:

1. Robert Munning Schmidt, Georg Schitter, Adrian Rankers, Jan van Eijk, „The Design of High Performance Mechatronics: High-Tech Functionality by Multidisciplinary System Integration, Delft Uni. press, 2020.
2. Hassan K. Khalil, „Nonlinear Control", Pearson, 2019.
3. Norman S. Nise, „Control Systems Engineering", Wiley, 2015.
4. Karl Astrom, Richard Murray, „Feedback Systems: An Introduction to Scientists and Engineers", Princeton University Press, 2008.
5. W. Bolton, „Mechatronics: Electronic Control Systems in Mechanical and Electrical Engineering", Pearson Education, 2003.
6. Mark Spong, Seth Hutchinson, M. Vidyasagar, „Robot Modeling and Control", Wiley, 2006.

<Course Code>					Linear Algebra and Optimization					
Teaching Scheme					Examination Scheme					
L	T	P	C	Hrs/Week	Theory			Practical		Total Marks
					MS	ES	IA	LW	LE/Viva	
3	0	0	3	3	25	50	25	--	--	100

COURSE OBJECTIVES

- To develop a deep understanding of fundamental concepts in linear algebra.
- To understand a deep understanding of fundamental concepts in optimization.
- To gain proficiency in translating real-world problems into mathematical models.
- To acquire knowledge about algorithms related to linear programming & optimization.

UNIT-1: VECTOR SPACE (11 Hrs)

Vector spaces and subspaces, Linearly independence, Bases and dimension of a vector space, Matrices, Rank, Change of basis, Inner product, norm, Gram-Schmidt process. Linear transformations.

UNIT-2: EIGEN VALUE AND EIGEN VECTORS (10Hrs)

Determinates, Eigenvalues and eigenvectors, Diagonalization, Eigenvectors and linear transformations, Complex eigenvalues, Singular value decomposition, and QR decomposition.

UNIT-3: UNCONSTRAINTOPTIMIZATION (10 Hrs)

Necessary and sufficient conditions for optima, convex sets, convex functions, optima of convex functions, steepest descent, Newton and Quasi-Newton methods, conjugate direction methods.

UNIT-4: CONSTRAINEDOPTIMIZATION (11 Hrs)

Constrained optimization - linear and non-linear constraints, equality and inequality constraints, optimality conditions, constrained convex optimization, projected gradient methods, and penalty methods.

Max. Hrs. 42

COURSE OUTCOMES

On completion of the course, the student will be able to:

CO1: Understand fundamental principles in linear algebra and optimization.

CO2: Apply mathematical modeling techniques to real-world problems and formulating solutions.

CO3: develop problem-solving skills and analytical thinking to analyze complex systems

CO4: analyze systems for linear and non-linear constraints in optimization

CO5: evaluate different types of optimization, both unconstrained and constrained.

CO6: create problem designs using the fundamentals of linear algebra and optimization.

TEXT/REFERENCE BOOKS

1. S. Axler, linear algebra done right, 2nd edn., springer, 1997.
2. E. K. P. Chong and s. H. Zak, an introduction to optimization, 2nd ed., wiley india pvt. Ltd., 2010.
3. G. Strang, linear algebra and its applications, nelson engineering, 2007.
4. D. C. Lay, linear algebra and its applications, 3rd ed., pearson, 2002.
5. D. G. Luenberger and y. Ye, linear and nonlinear programming, 3rd ed, springer, 2010.